

**REMARKS**

This amendment accompanies a Request for Continued Examination, and is responsive to the Final Office Action mailed November 29, 2002. Claims 27-45 are pending. Claims 37-38 have been amended, and claims 39-45 have been newly added. Reconsideration is respectfully requested.

**1. Rejection of Claims 37-38 Under § 112**

Claims 37-38 were rejected under 35 U.S.C. 112 second paragraph as being indefinite for failing to provide adequate antecedent basis.

Claims 37-38 have been amended to correct this informality. Claims 37-38 now properly make reference to the "upper" portion of the source region, and not the "second" region thereof.

**2. Rejection of Claims 27-30 and 37 Under § 102(b)**

Claims 27-30 and 37 were rejected under 35 U.S.C. 102(b) as being anticipated by USP 5,939,749 (Taketa). The Applicants respectfully traverse this rejection.

Claim 27 recites that the floating gate consists of first and second portions integrally formed together, where the conductive source region upper portion is disposed over and insulated from the floating gate first portion *and not the floating gate second portion*, and the control gate second portion is disposed over and insulated from the floating gate second portion *and not the floating gate first portion*. Thus, no matter how one divides the floating gate into the integrally formed together first and second portions, no portion of the claimed floating gate can have both the source region upper portion and the control gate second portion disposed over it. In contrast, Taketa teaches that the control gate is disposed over part (see Fig. 6) or all (see Fig. 1) of the floating gate 32, and the upper portion of the source electrode 14 is disposed over both the control gate 9 and the floating gate 32. Therefore, there are no first and second integrally formed together portions of floating gate 32 of Taketa that satisfy the limitations of claim 27.

On page 9 of the Final Office Action, the Examiner states that the Taketa floating gate 32 illustrated in Fig. 6 has first and second integrally formed floating gate portions that meet the limitations recited in claim 27. Yet, the Examiner fails to explain with any specificity how the

floating gate of Taketa can be divided into first and second integrally formed together portions in a manner that meets the claim limitations of claim 27. If the Examiner maintains this rejection, clarification is respectfully requested.

It is therefore submitted that Taketa does not anticipate claim 27 (and claims 28-30 and 37 dependent thereon). Moreover, Taketa fails to teach all the elements of these dependent claims as well. For example, claim 37 as amended recites the insulation material disposed between the source region upper portion and the floating gate first portion has a thickness for permitting voltage coupling therebetween. In contrast, the portion of source electrode 14 disposed over floating gate 32 in Taketa not only extends over spacer 15 or 61, but also extends over control gate 9, clearly precluding voltage coupling between that portion of the source electrode 14 and the floating gate 32.

### **3. Rejection of Claims 31-36 and 38 Under § 103(a)**

Claims 31-36 and 38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Taketa in view of USP 6,211,547 (Kao).

Claim 31 recites memory cell pairs formed with the same essential features as those recited in claim 27, including the floating gates (each consisting of a first portion and a second portion integrally formed together) where the electrically conductive source region upper portion is disposed over and insulated from the floating gate first portions *and not the floating gate second portions*, and each of the pair of electrically conductive control gates are adjacent one of the floating gates and each has a second portion disposed over and insulated from the second portion *and not the first portion* of the one floating gate. For the reasons set forth above in Part 2, it is respectfully submitted that Taketa fails to teach or suggest the memory device array as recited in claim 31. Furthermore, it is submitted that the addition of Kao fails to remedy the deficiencies of the Taketa reference.

It is therefore submitted that claim 31, along with claims 32-36 and 38 dependent thereon, are allowable over the combination of Taketa and Kao references. Moreover, the combination of Taketa and Kao fails to teach all the elements of these dependent claims as well. For example, claim 38 as amended recites the insulation material disposed between the source

region upper portion and each of the floating gate first portions has a thickness for permitting voltage coupling therebetween. As stated above, the portion of source electrode 14 disposed over floating gates 32 of Taketa not only extends over spacer 15 or 61, but also extends over control gate 9, clearly precluding voltage coupling between that portion of the source electrode 14 and the floating gates 32.

#### 4. New Claims

Claims 39-45 have been newly added. Claims 39 and 42 essentially recite the memory device structure of claims 27 and 31, and further recite that the source region upper portion is disposed adjacent to and insulated from the second control gate portion, with no vertical overlap therebetween. It is respectfully submitted that Taketa and/or Kao fail to teach or suggest such a memory device structure.

Allowance of the newly added claims is respectfully requested.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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